UG Odd Semester (Old) Exam., December—2016

COMPUTER SCIENCE

(1st Semester)

Course No. : CS–102 (O)

(Digital Electronics and Fundamentals of Computer)

Full Marks : 75
Pass Marks : 26

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **five** questions, selecting **one** from each Unit

UNIT—I

1. *(a)* Write the characteristics of digital ICs. 8

(b) Describe various types of multivibrators. 7

2. *(a)* Convert the following number from the given base to the base indicated : 8

(i) Decimal 41·6875 to binary

(ii) Decimal 153·513 to octal

(iii) Octal 673·124 to hexadecimal

(iv) 10110001101011 to octal

(b) Explain the logical operations AND, OR and NOT. 7

UNIT—II

3. *(a)* Express the following function in sum of minterms and product of maxterms : 6

$F(A, B, C, D)$ $D(A$ $B)$ $B\,D$

(b) Explain NOR and NAND operation. 4

(c) Simplify the following Boolean functions to a minimum number of literals : 5

(i) xy xy

(ii) $y(wz$ $wz)$ xy

4. *(a)* Prove De Morgan's theorem using truth table. 7

(b) Simplify the following Boolean function F in sum of products using don't care condition : 8

(i) F $B\,C\,D$ BCD $ABCD$
d $B\,CD$ $A\,BC\,D$

(ii) F $W\,(x\,y$ $x\,y$ $xyz)$ $x\,z\,(y$ $w)$
d $W\,x(y\,z$ $yz\,)$ xyz

UNIT—III

5. *(a)* Design a combinational circuit whose input is a 4-bit number and whose output is the 2's complement of the input number. 9

(b) What is multiplexer? Implement the following function with an 8 1 multiplexer : 1+5=6

$F(A, B, C, D)$ (0, 1, 3, 4, 8, 9, 15)

6. *(a)* What is decoder? A combinational circuit is defined by the following three functions :

F_1 $x\,y$ xyz
F_2 x y
F_3 xy $x\,y$

Design the circuit with decoder and external gates. 1+7=8

(b) Implement a full-adder with two half-adders and an OR gate. 7

UNIT—IV

7. *(a)* Explain master-slave *J-K* flip-flop. 5

(b) What is flip-flop excitation table? Write the excitation table and characteristic table of *R-S* flip-flop. 5

(c) Reduce the number of states in the following state table and show the reduced state table : 5

	Next State		*Output*	
Present State	*X* 0	*X* 1	*X* 0	*X* 1
a	*f*	*b*	0	0
b	*d*	*c*	0	0
c	*f*	*e*	0	0
d	*g*	*a*	1	0
e	*d*	*c*	0	0
f	*f*	*b*	1	1
g	*g*	*h*	0	1
h	*g*	*a*	1	0

8. *(a)* Using *J-K* flip-flop, design a binary counter having the following repeated binary sequence : 8

0, 1, 2, 3, 4, 5, 6

(b) Write the procedure for the design of sequential circuits. 7

UNIT—V

9. *(a)* Design a 4-bit ripple counter. 8

(b) What is shift register? The content of a 4-bit shift register is initially 1101. The register is shifted six times to the right, with the serial input being 101101. What is the content of the register after each shift? 2+5=7

10. Write short notes on the following : 5×3=15

(a) Programmable logic array (PLA)

(b) Magnetic-core memory

(c) RAM

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