# 2016/ODD/12/33/ETC–703/618

**B.Tech Odd Semester (CBCS) Exam.,**
**December—2016**

## ELECTRONICS AND TELECOMMUNICATION ENGINEERING

**( 7th Semester )**

Course No. : ETC-703D

**( EDA for VLSI Design )**

*Full Marks* : 75
*Pass Marks* : 30

*Time* : 3 hours

*Note* : 1. Attempt **five** questions, selecting **one** from each Unit.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the margin indicate full marks for the questions.

### UNIT—I

**1.** *(a)* Discuss the evolution of VLSI technology. State the Moore's law. 3+2=5

*(b)* What are different VLSI design styles? Explain each of them in detail. 10





**2.** *(a)* Draw the VLSI design flow and explain each step. 10

*(b)* What do you mean by electronic design automation? Explain. 5

### UNIT—II

**3.** *(a)* Write a VHDL program to design a 4:1 multiplexer using dataflow modelling style. 5

*(b)* Write a VHDL program to design a positive edge triggered D flip-flop. 5

*(c)* Write a VHDL program to design a full-adder using two half-adders as component. 5

**4.** *(a)* Write a VHDL program to design a 4-bit shift register with a capability of serial-in serial-out data shift. 10

*(b)* What are different modelling styles in VHDL programming? Explain in brief. 5

### UNIT—III

**5.** *(a)* Draw the architecture of a CPLD and explain its working principle. 10

*(b)* Draw a typical macrocell architecture and explain. 5

**6.** (a) What is the concept of LUT in FPGA? What do you mean by switch matrix and configurable logic block in FPGA? 2+4=6

(b) Draw the architecture of a Xilinx FPGA and explain its working principle. 9

UNIT—IV

**7.** (a) What is consensus theorem? Draw the ROBDD of the following Boolean expression : 2+8=10

$$Y \quad A\overline{B}C \quad B\overline{C} \quad ABC$$

(b) What are the different functions you can design using two input variables? 5

**8.** (a) Explain the steps of designing sequential logic circuits. 6

(b) What is state minimization technique? 4

(c) What do you mean by static timing analysis? 5

UNIT—V

**9.** (a) What are different fault models? Why is VLSI testing an important step in VLSI circuit design? 5+5=10

(b) Draw and explain the architecture of boundary scan test circuit. 5





**10.** (a) What is the meaning of physical verification in VLSI design? 4

(b) What is the yield of VLSI circuit? 3

(c) What is IDDQ test? 3

(d) How do you overcome the electro-migration problem of the VLSI circuit? 5

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