B.Tech Odd Semester (CBCS) Exam.,
December—2016

ELECTRONICS AND COMMUNICATION ENGINEERING

(3rd Semester)

Course No. : ECCC–01

(Digital Electronics Circuits)

Full Marks : 50
Pass Marks : 15

Time : 2 hours

Note : 1. Answer *any* **five** questions.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the margin indicate full marks for the questions.

1. *(a)* Perform the following decimal additions in the 8421 code : 2

(i) 25   13

(ii) 679 6   536 8

(b) Convert the following decimal numbers to their binary equivalent : 2

(i) $(83)_{10}$

(ii) $(79\ 515)_{10}$

(c) Find the minterms for the function

$$Y(A, B, C) \quad AB \quad ABC \quad B$$ 2

(d) Minimize the Boolean expression using K-map : 4

$$Y(A, B, C) \qquad (1, 3, 5, 7)$$

2. *(a)* Explain CMOS inverter gate with a circuit diagram. 4

(b) Explain the working of a two-input TTL NAND gate with the help of a circuit diagram. 4

(c) Explain the following parameters : 2

(i) Noise margin

(ii) Propagation delay

3. *(a)* Design a combinational logic circuit with three input variables that will produce logic 1 output when more than one variables are logic 1. 5

(b) Design an 8 : 1 multiplexer using NAND gates only. 5

4. *(a)* Implement the following function using 3 to 8 line decoder : 5

$$Y(A, B, C) \qquad (0, 1, 5, 6)$$

(b) Implement the following function using s multiplexer : 5

$$Y(A, B, C) \qquad m(1, 2, 5, 6)$$

5. *(a)* Draw the logic circuit of S-R flip-flop using D flip-flop. 6

(b) Explain J-K flip-flop with logic diagram. 4

6. *(a)* What is race around condition? How does it get eliminated in a master-slave J-K flip-flop? Explain. 5

(b) Design a circuit to generate the sequence 0 2 5 4 7 3. 5

7. *(a)* Differentiate between static RAM and dynamic RAM. 5

(b) Explain the classification of memory chip. 5

8. *(a)* What is CLB? What are the components of a simple Xilinx FPGA? 5

(b) Explain the block diagram of PLA in detail. 5

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