B.Tech Odd Semester (CBCS) Exam., 2016

ELECTRONICS AND COMMUNICATION ENGINEERING

(3rd Semester)

Course No. : EC–CF–05

(Circuit Theory and Network Analysis)

Full Marks : 50
Pass Marks : 15

Time : 2 hours

Note : 1. Attempt *any* **five** questions.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the margin indicate full marks for the questions.

1. *(a)* Determine the current through R 3 resistor for the circuit shown in Fig. 1 below using superposition theorem : 5

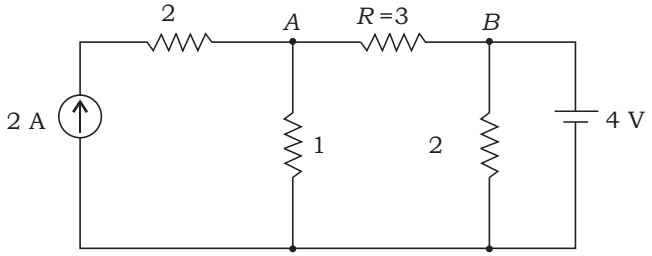

Fig. 1

(b) Find the value of R_L for maximum power transfer and also the maximum power shown in Fig. 2 below : 5

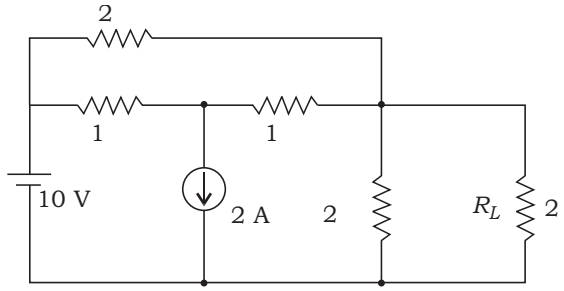

Fig. 2

2. *(a)* From the following figure (Fig. 3)

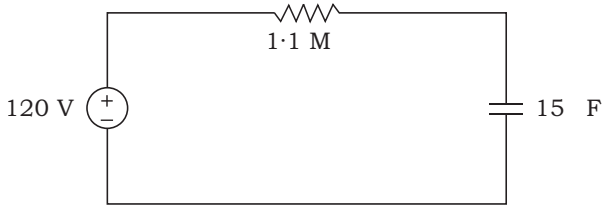

Fig. 3

calculate—

(i) the time constant of the circuit;

(ii) the initial value of charging current;

(iii) the initial rate of rise of voltage across the capacitor;

(iv) the voltage across the capacitor after a time equal to the time constant;

(v) the current at a time equal to the time constant of the circuit. 5

(b) In the circuit shown below in Fig. 4, the switch K is thrown from position A to position B at time t 0, the current is previously reached its steady-state. Determine $i(t)$ after switching : 5

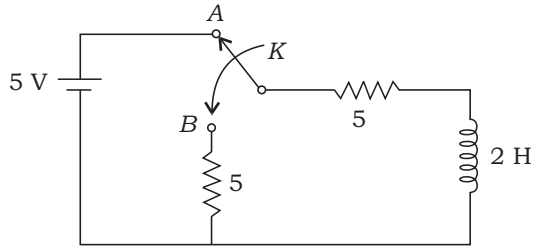

Fig. 4

3. *(a)* An *R-L-C* series circuit has R 1 k , L 100 mH, C 10 F. If a voltage of 100 is applied across the series combination, determine—

(i) resonant frequency;

(ii) Q factor;

(iii) half-power frequencies. 5

(b) Synthesize the *R-L* driving point impedance

$$Z(s) \quad \frac{2(s \ 1)(s \ 3)}{(s \ 2)(s \ 6)}$$

to get—

(i) the Foster first form;

(ii) the Cauer second form of realization. 5

4. For the network shown in Fig. 5 below

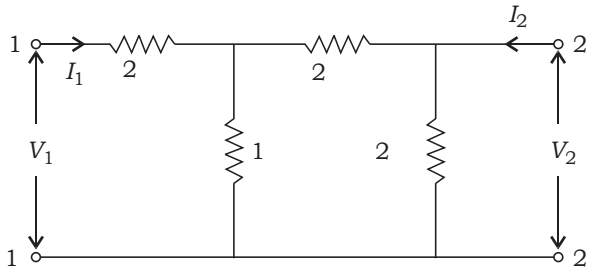

Fig. 5

(a) derive the open-circuit impedance parameters and draw its equivalent circuit;

(b) derive the short-circuit admittance parameters and draw its equivalent circuit. 5+5

5. *(a)* Draw the directed graph of the network shown in Fig. 6 below :

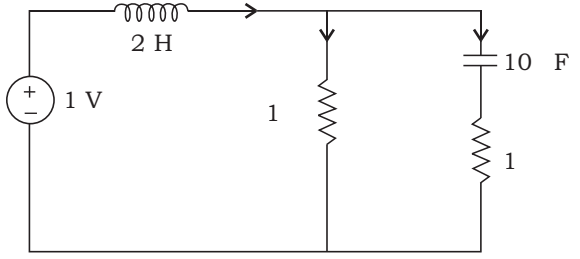

Fig. 6

For the same graph, write the incidence matrix A, cut-set matrix B and loop matrix C. 5

(b) Draw the dual of the network shown in Fig. 7 below : 5

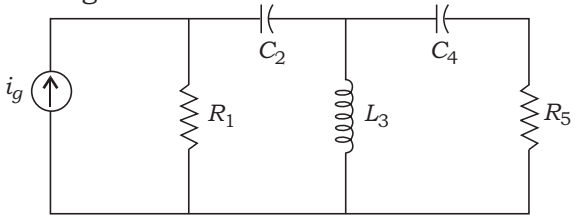

Fig. 7

6. *(a)* The switch S is closed at t 0. If capacitor is initially uncharged, find the currents $i_1(t)$ and $i_2(t)$ for the circuit shown in Fig. 8 below : 5

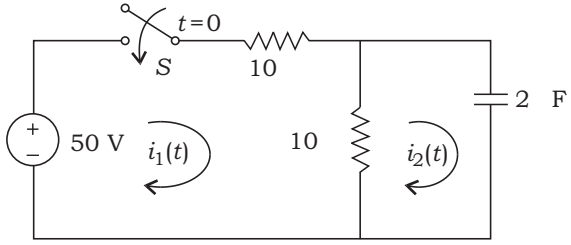

Fig. 8

(b) Determine the mesh currents of the network shown in Fig. 9 below by mesh analysis : 5

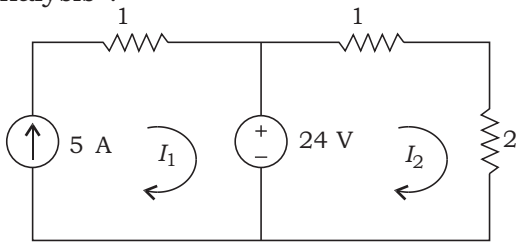

Fig. 9

7. *(a)* For the circuit shown in Fig. 10 below, find the Rth and Vth at terminal a to b : 6

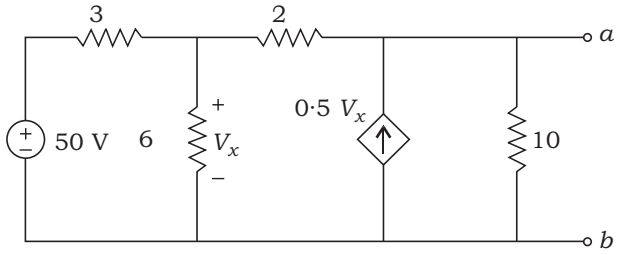

Fig. 10

(b) Use Delta-Y transformation to determine the resistance between A and B of the network shown in Fig. 11 below : 4

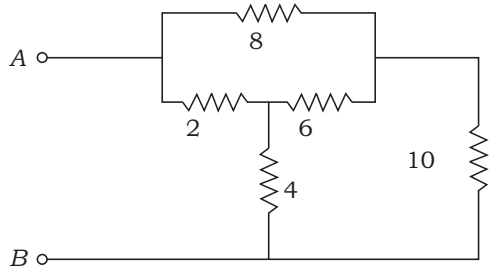

Fig. 11

8. *(a)* For the circuit shown in Fig. 12 below find the current I : 5

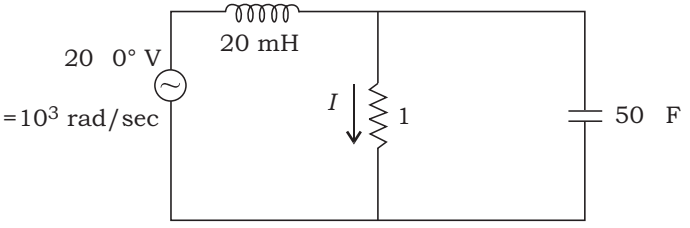

Fig. 12

(b) For the circuit shown in Fig. 13 below, if V_s $6u(t)$ and $V_o(0)$ 1 V, then find $V_o(t)$ for t 0 : 5

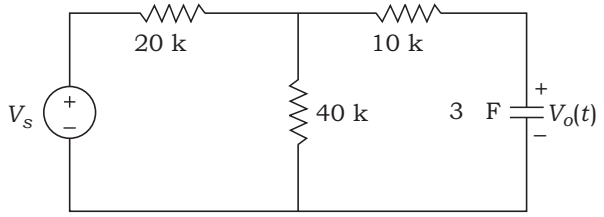

Fig. 13

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