2016/ODD/12/33/ETC–504/614

B.Tech Odd Semester (CBCS) Exam., December—2016

ELECTRONICS AND TELECOMMUNICATION ENGINEERING

(5th Semester)

Course No. : ETC–504

(Digital VLSI Design)

Full Marks : 75

Pass Marks : 30

Time : 3 hours

Note : 1. Attempt **one** question from each Unit.
2. Begin each answer in a new page.
3. Answer parts of a question at a place.
4. Assume reasonable data wherever required.
5. The figures in the margin indicate full marks for the questions.

UNIT—I

1. *(a)* Derive the drain current of MOS device in different operating regions. 8

(b) Explain the operations of NMOS enhancement and depletion transistors. 7

2. *(a)* List the basic process for IC fabrication. 2

(b) With neat diagram, explain the n-well and channel formation in CMOS process. 10

(c) Compare nMOS and pMOS transistors. 3

UNIT—II

3. *(a)* Design a static CMOS circuit to implement the following Boolean functions : 3+3=6

(i) $F \quad D\,E\,A \quad B\,C$

(ii) $F \quad (\overline{W \quad XY \quad Z})$

(b) Realize a 2 : 1 MUX using CMOS transmission gate and explain its operation. 5

(c) Realize the following Boolean function using pseudo-nMOS logic : 4

$$Y \quad A \odot B \odot C$$

4. *(a)* Explain, why NAND is preferred over NOR gate using the concept of logical effort. 5

(b) Design a two-input XOR gate using CMOS transmission gate and explain its operation. 5

(c) Implement the Boolean function

$$Y \quad [\overline{A(B \quad C) \quad DE}]$$

using static CMOS with minimum number of transistor. 5

UNIT—III

5. (a) What is stick diagram? What are the uses of stick diagram? 1+2=3

(b) Develop the necessary stick diagram and lay out for the designs of inverter, NAND and NOR gates. 12

6. (a) What do you mean by design rules? Discuss different design rules with examples. 10

(b) Sketch the stick diagram for two-input XOR gate. 5

UNIT—IV

7. (a) Draw and explain the MOS C-V characteristics. 6

(b) Discuss various MOSFET capacitances. 9

8. (a) Calculate the propagation delay of the CMOS inverter. 6

(b) Calculate the dynamic power dissipation of a CMOS inverter

operating at 2·62 MHz. The power supply voltage is 1·8 V and the load capacitance is 10 fF. If the delay through the inverter is 10 ps, then calculate the power delay product (PDP). 4

(c) Explain briefly about the short-channel effect of MOS device. 5

UNIT—V

9. (a) Design a T flip-flop using static CMOS and transmission gate. 5

(b) Design the following logic using domino CMOS logic and compare it with the static CMOS logic : 5

$$Y \quad AB \quad CD \quad EFG$$

(c) Design a BiCMOS two-input NAND logic and explain its operation. 5

10. (a) Briefly explain the six-transistor SRAM architecture and its operational mechanism. 6

(b) Draw the circuit of CMOS full-adder circuit and explain its operation. 6

(c) What are the advantages and disadvantages of dynamic CMOS over static CMOS? 3

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