# UG/PG ODD SEMESTER EXAMINATION, 2022

## COMPUTER SCIENCE

1st Semester

Course No. : MCSC-103

**(Digital Logic and Switching Theory)**

Full Marks : 70

Pass Marks : 28

Time : 3 hours

*The figures in the margin indicate full marks for the questions*
*Answer five questions, taking one from each unit.*

## UNIT-I

1. (a) Convert:

(i) $(724)_{10}$ to binary, octal, and hexadecimal numbers. 3

(ii)$(10101110001111)_2$ to octal and hexadecimal numbers using the group method. 2

(iii) $(FACE)_{16}$ to binary numbers. 1

(b) Perform the binary operations:

(i) 1101100 + 101011 1

(ii) 1011100 - 011010 using 2's complement method. 2

(c) Simplify F(x,y,z)= Σ(0,1,6,7) using K-map. 2

(d) Draw the NOR implementation of F=xy+yz. 3

2. (a) Convert:

(i) $(69BF)_{16}$ to binary and octal numbers. 2

(ii) $(138)_{10}$ to binary and hexadecimal numbers. 2

(b) Subtract 11100-10000 using 1's complement method and verify. 2

(c) Simplify 2+2=4

(i) F=xyz+xyz'+xy

(ii) F=xy+xyz+yz

(d) Prove De-Morgan's law. 4

## UNIT-II

3. (a) Design: 3+3=6

i) Half adder circuit

ii) Full subtractor circuit

(b) What are the uses of MUX circuit in communication? 2

(c) Compare combinational circuits and sequential circuits. 2

(d) Draw the diagram of binary parallel adder and explain. 4



## UNIT-V

9. (a) A combinational circuit is defined by the functions : 9

F1(A, B, C) = Σ (3, 5, 6, 7)

F2(A, B, C) = Σ (0, 2, 4, 7)

Implement the circuit with a PLA having three inputs, four products terms and two outputs.

(b) Simplify the boolean function using k-map in SOP and POS forms and implement with gates. 5

F(x, y, z) = Σm(0, 2, 3, 4, 5, 6)

10. (a) Design a PROM circuit using OR gate, followed by AND gate and buffer for the following expression. 8

$F_1$ (x, y, z) = Σm(0, 1, 3, 5, 7)

$F_2$ (x, y, z) = Σm(1, 2, 5, 6)

(b) Write short notes on the following :3x2=6

(i) Programmable logic Device

(ii) Threshold functions.

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4. (a) Design: 3+3=6

(i) Full adder circuit

(ii) Half subtractor circuit

(b) Subtract 1110-1000 using the circuit of full subtractor and show the signal flow. 4

(c) Compare encoder and decoder. 2

(d) Draw a circuit to make 8×1 MUX using 2×1 MUX 2

## UNIT-III

5. (a)(i) Draw the logic diagram for BCD-to-excess-3 code converter.

(ii) What are the steps to be followed to obtain the output boolean functions from a logic diagram. 2+4=6

(b) Obtain the NAND logic diagram of a full-adder from the Boolean functions : 8

$C = xy + xz + yz$

$S = C' (x+y+z) + xyz$

6. (a) Draw the logic diagram of a 3-to-8 line decoder with the truth table. 6

(b) Implement the given function with a multiplexer. 6

$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$

(c) How many don't care inputs are there in a BCD adder? 2





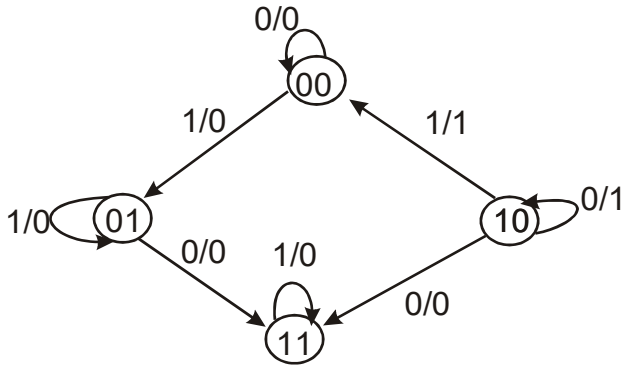
## UNIT-IV

7. (a) Differentiate between combinational circuit and sequential circuit. 3

(b) Write the steps to design a synchronous sequential circuit. 8

(c) Distinguish between serial binary adder and parallel binary adder. 3

8. (a) Considering the state diagram




Find the following : 9

(i) State table

(ii) Number of states

(iii) Type of flip-flop used

(iv) Circuit excitation table

(v) Obtain Boolean Expression

(b) Show the logic diagram of a clocked D flip-flop with AND and NOR gates. 5