PG Odd Semester (CBCS) Exam., December—2017

PHYSICS

(1st Semester)

Course No. : PHYCC–104

(Electronics)

Full Marks : 70
Pass Marks : 28

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **five** questions, selecting **one** from each Unit

UNIT—I

1. *(a)* Draw the circuit diagram of a full-wave rectifier and explain its working. Obtain the expression for its efficiency and ripple factor. 4+6=10

(b) Discuss the application of diode as positive and negative clippers. 2+2=4

2. *(a)* Discuss the construction and working principle of *n*-channel FET. Deduce the relation $g_{m\ d}$ for FET (where the symbols have their usual meanings). 4+3=7

(b) Discuss the role of Zener diode as voltage regulator. 4

(c) The following readings were obtained experimentally from a JFET :

V_{GS}	0 V	0 V	0·3 V
V_{DS}	5 V	10 V	10 V
I_D	8 mA	8·2 mA	7·6 mA

Determine—

(i) a.c. drain resistance;

(ii) transconductance;

(iii) amplification factor. 3

UNIT—II

3. *(a)* Obtain an expression for the gain of an amplifier using negative feedback. Discuss the effect of negative feedback in an amplifier on its—

(i) input impedance;

(ii) output impedance;

(iii) bandwidths. 3+2+2+2=9

(b) Describe the working of phase-shift oscillator with appropriate circuit diagram. 5

4. *(a)* Write in brief on the following : 3+3=6

(i) LED

(ii) Solar cell

(b) Discuss the construction and working of UJT (unijunction transistor). How can it be used as an oscillator? 6

(c) State and explain Barkhausen criterion. 2

UNIT—III

5. *(a)* Discuss the application of Op-Amp as—

(i) inverting amplifier;

(ii) integrator;

(iii) voltage comparator. 2+2+3=7

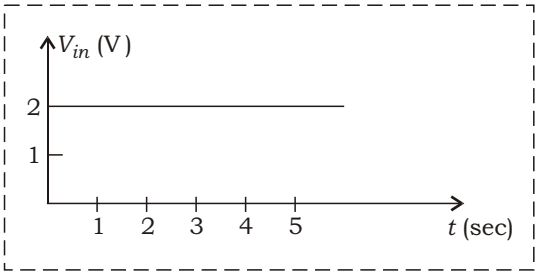
(b) Define CMRR. Why is CMRR kept high in design of differential amplifier? 4

(c) Discuss slew rate of an Op-Amp. 3

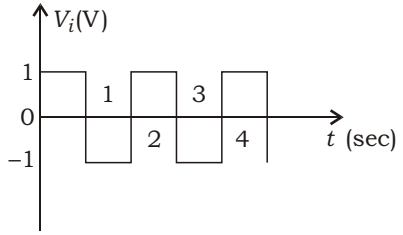
6. *(a)* Discuss Op-Amp as *(i)* low-pass and *(ii)* high-pass active filters. 3+3=6

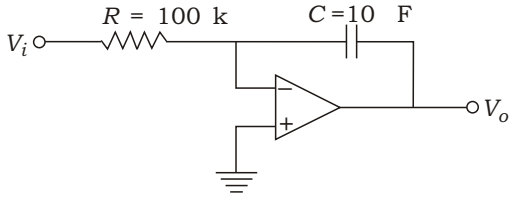
(b) What are the characteristics of an ideal Op-Amp? 2

(c) Determine the output of an integrator if the input is a step (d.c.) voltage as (Assume RC 1) shown below. Draw the output waveform : 3



(d) Find the output voltage (V_0) for the input voltage (V_i) : 3





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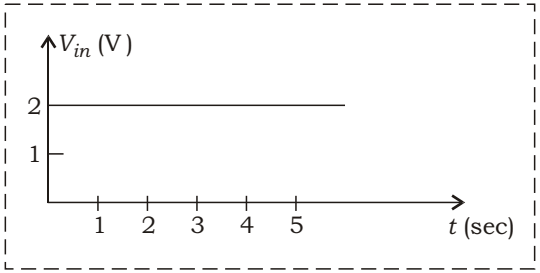

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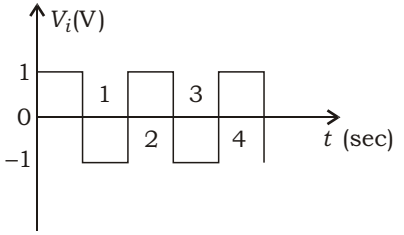

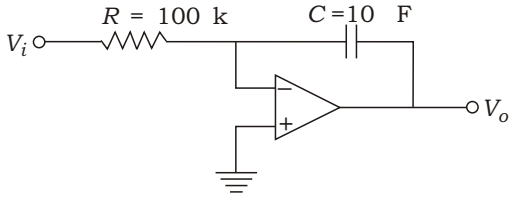

UNIT—IV

7. *(a)* Explain the working of AND and NOT gates with their circuit diagrams (discrete components), Boolean expression and truth table. 4+4=8

(b) Simplify : 2+2+2=6

(i) $Y \quad AB \quad ABC \quad \overline{A}B \quad A\overline{B}C$

(ii) $Y \quad (A \quad B \quad C)\,(A \quad B)$

(iii) $Y \quad \overline{(A \quad \overline{B} \quad C) \quad (B \quad \overline{C})}$

8. *(a)* Discuss *R-S* latch using NAND gate. 5

(b) What is race condition in *R-S* latch? Show how it is removed in *D*-latch. 1+2=3

(c) What is the simplified Boolean equation for the following logic equation expressed by minterms?

$Y \quad F(A, B, C, D)$

$m\,(7, 9, 10, 11, 12, 13, 14, 15)$ 6

UNIT—V

9. *(a)* Define amplitude modulation. Derive the voltage equation of an AM wave. What are the sideband frequencies? 1+4+2=7

(b) Discuss the advantages of FM over AM. 3