B.Tech Even Semester Examination, May, 2025

Computer Science & Engineering

(4th Semester)

Course No: CSE-254/CSE-402

(Computer Organisation and Architecture)

Full Marks: 70
Pass Marks: 28
Time: 3 hours

Note:

1. Attempt any five questions taking one each unit.
2. Begin each answer in a new page
3. Answer parts of a question at a place
4. Assume reasonable data wherever required
5. The figure in the right margin indicates full marks for the question
6. All the mathematical symbols and abbreviations have their usual meanings.

UNIT-I

1. (a) Discuss five different addressing modes used in MIPS 32-bit architecture. [10]

   (b) Convert the following C code into MIPS assembly code:

```
while (a < 10) {
        D[a] = b + a;
        a = a + 1;
        }
```

[4]

2. (a) Discuss the basic operational concept of an instruction [5]

   (b) Write the MIPS assembly code for the following recursive procedure that calculates factorial:

```
int fact(int n) {
        if (n < 1) return 1;
        else return n * fact(n - 1);
        }
```
[9]

UNIT-II

3. Explain, with a diagram, the shift-and-add version of multiplication where the Multiplicand and Product registers are 2n bits wide and the Multiplier register is n bits wide. Given the multiplier is 0011 and the multiplicand is 0010, describe the step-by-step process of how the product is calculated using this method. [8+6]

4. (a) Given the following CPIs for instruction classes:

Class	CPI
Class A	1
Class B	2
Class C	3

Sequence	Class A	Class B	Class C
1	2	1	2
2	4	1	1

i. Which sequence executes the most instructions?

ii. Which sequence is faster?

iii. What is the CPI for each sequence? [5]

(b) Derive the expressions for the **generate** and **propagate** signals, as well as the carry signals for a 4-bit **carry-lookaheadadder**. Additionally, explain the advantages of using a carry-lookahead adder over a **ripple carry adder** in terms of **propagation delay**.
[3+4+2]

The individual stages of the data path have the following latencies:

IF	ID	EX	MEM	WB
250ps	350ps	150ps	300ps	200ps

(i) What is the clock cycle time in a pipelined processor?

(ii) What is the total latency of an LW instruction in a pipelined processor?
[2+3]

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I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
200 ps	70 ps	20 ps	90 ps	90 ps	250 ps	15 ps	10 ps

(i) If a processor only needs to fetch consecutive instructions , what would be the **cycle time**?

(ii) If the processor must support only **conditional PC-relative branches**. What would be the **cycle time**?

(iii) If the processor must support only **R-type of instruction** . What would be the **cycle time**? [2+2.5+2.5]

9. Define different Hazards in pipeline architecture [6]

. Consider the following MIPS assembly code: [2+3+3]

```
sub   $2, $1, $3
and   $12, $2, $5
or    $13, $6, $2
add   $14, $2, $2
sw    $15, 100($2)
```

(i) Identify the data hazards present in this sequence of instructions.

(ii) Explain how **forwarding** can be used to resolve the data hazards in this sequence.

(iii) Which method, forwarding or reordering, is more effective in this case, and why? [2+3+3]

10. Draw the **data path** for a **pipelined MIPS architecture**. Then, calculate, with an explanation, the size of the different **pipelined registers** in your architecture, excluding the control signals. [3+6]

UNIT-III

5. (a) Explain the design and working of a SRAM memory. Write SRAM vs DRAM [7+3]

(b) How many total bits are required for a direct-mapped cache with 16 KiB of data and 4-word blocks, assuming a 32-bit address? [4]

6. (a) .What is cache memory? Define and explain direct-mapped cache, set associative cache . [2+6]

(b) Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 100 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%. [6]

7. (a) What is a **data path element** in a processor? Design the **data path** for an R-type instruction in a MIPS architecture and explain its working. [2+4+3]

(b) Write short notes on register file. [5]

UNIT-IV

8. (a) Discuss the different **control signals** in the **MIPS non-pipelined architecture** and explain their roles in the execution of instructions. [7]

(b) The latencies of the following logic blocks are given in the table: [