M.Tech Even Semester Examination, May, 2025

Electronics & Communication Engineering

(2nd Semester)

Course No: MECE-201

(Analog VLSI Design)

Full Marks: 70

Pass Marks: 28

Time: 3 hours

Note:

1. Attempt any five questions taking one from each unit.
2. Begin each answer in a new page
3. Answer parts of a question at a place
4. Assume reasonable data wherever required
5. The figure in the right margin indicates full marks for the question
6. All the mathematical symbols and abbreviations have their usual meanings.

UNIT-I

1. Differentiate enhancement mode and depletion mode MOSFET? Derive the MOS diffusion capacitance model. 4+10=14

2. Discuss how the body effect influences the threshold voltage of a MOSFET? Explain the effect of substrate doping and oxide thickness on the Body Effect in a MOS transistor. 4+10=14

UNIT-II

3. Discuss the fabrication steps involved in N-well and P-well CMOS devices. Discuss the Euler path technique used in layout design. 7+7=14

4. What is Cascode current mirror? Discuss the working principle of a Cascode current mirror, with proper circuit diagram 4+10=14

UNIT-III

5. What is triode load? Discuss the MOS common source amplifier circuit with (a) triode connected load (b) Current-source load. 2+6+6=14

6. Explain the working principle of a MOSFET differential amplifier with diode connected active load. Discuss how a current mirror can be used as a load. 7+7=14

UNIT-IV

7. Design a Two stage Folded Cascode OP-amp circuit and discuss its working principle. Comment on the stability and phase compensation techniques related to OP-amp. 5+5+4=14

8. Design a high-speed and highly-linear CMOS sample and hold circuit that can be used with an ADC circuit. 14

UNIT-V

9. Discuss Switched capacitor integrators? Explain the working principle of CMOS voltage controlled oscillators. 4+10=14

10. What is over-sampling? Design a flash ADC convertor and explain its working principle. 2+12=14

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