2017/ODD/18/24/MCS–103/354

UG Odd Semester (CBCS) Exam., December—2017

COMPUTER SCIENCE

(1st Semester)

Course No. : MCSCC–103

(Digital Logic and Switching Theory)

Full Marks : 70
Pass Marks : 28

Time : 3 hours

The figures in the margin indicate full marks for the questions

Answer **five** questions, selecting **one** from each Unit

UNIT—I

1. *(a)* Define digital computer. 1

(b) Convert $(10101100)_2$ to octal, decimal and hexadecimal numbers. 3

(c) Subtract $(1100)_2$ $(1010)_2$ using 2's compliment method. 2

(d) Represent 235 in Excess-3 code. 2

(e) Prove De Morgan's law of Boolean variables. 4

(f) Simplify $xy \quad xy$. 2

2. *(a)* Convert $(724)_{10}$ to binary, octal and BCD code. 3

(b) Subtract $(0011)_2$ $(1100)_2$. 2

(c) Subtract $(52)_{10}$ $(48)_{10}$ using 10's compliment and verify the answer in binary number system. 4

(d) Simplify $xyz \quad x\,y \quad xyz$. 2

(e) Simplify using K-map if

$$F(x, y, z) \qquad (0, 4, 2, 6)$$ 3

UNIT—II

3. *(a)* Explain half-adder and implement its circuit using NOR. 5

(b) Add $(0011)_2$ and $(1101)_2$ in a binary parallel adder circuit. 4

(c) Explain digital comparator with diagram. Put values to the inputs and show $A \quad B$, $A \quad B$ and $A \quad B$. 3

(d) Write the application of MUX in communication system. 2

4. *(a)* Explain half-subtractor and implement its circuits using NAND. 5

(b) Draw an adder-subtractor circuit and show the execution for both M 0 and M 1. 4

(c) Design a decoder with 3 inputs and 8(2^3) output signals. 3

(d) What is encoder? Why is it used? 2

UNIT—III

5. *(a)* What do you mean by finite state machine? 2

(b) Write down the applications of flip-flops. 3

(c) What is timing in sequential circuits? 2

(d) Explain *J-K* flip-flop. 4

(e) Compare *S-R* flip-flop and *S-R* latch. 3

6. *(a)* Define flip-flop. What are the broad categories of sequential circuits? Explain. 1+2=3

(b) Explain *R-S* flip-flop. 4

(c) Write the characteristic table of *T* flip-flop. 2

(d) Explain binary counter. 4

(e) What is edge-triggered flip-flop? 1

UNIT—IV

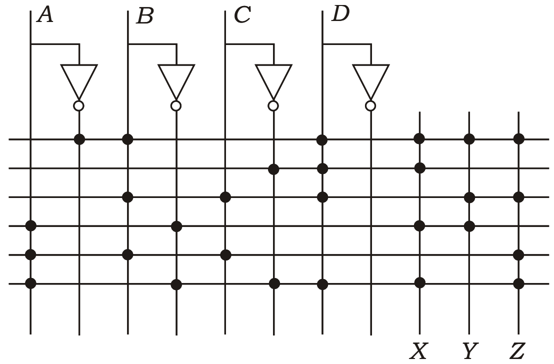
7. *(a)* Write the advantages and disadvantages of using ROM and PLA for combinational logic implementation. 6

(b) Implement

$$f_1(x_2, x_1) \quad m(0, 3)$$
$$f_2(x_2, x_1) \quad \overline{x_2 \quad x_1}$$
$$f_3(x_2, x_1) \quad M(1)$$

with a 4 3 ROM. 4

(c) The internal connection diagram for a PLA is given below. Write the equations realized the PLA : 4



8. *(a)* Draw the block diagram and explain Programmable Logic Array (PLA). 5

(b) Show how to program the fusible links to get a 4-bit gray code from the binary inputs using PAL. 9

UNIT—V

9. Design a digital system with two flip-flops, say B and C and one 4-bit binary counter A, in which the individual flip-flops are denoted by A_4, A_3, A_2, A_1. A start signal S initiates the system operation by clearing the counter A and flip-flop C and setting flip-flop B to one. The counter is then incremented by one starting from the next clock pulse and continues to increment until the operation stop. Counter bits A_3 and A_4 determine the sequence of operations :

If A_3 0, B is cleared to 0 and the count continues.

If A_3 1, B is set to 1; then A_4 0, the count continues, but if A_4 1, C is set to 1 on the next clock pulse and the system stops counting.

Then if S 0, the system remains in the initial state, but if S 1, the operation cycle repeats.

(a) Draw the ASM chart.

(b) Tabulate the timing sequence. 14

10. *(a)* Write the procedure for construction of ASM charts with an example. 5

(b) Derive the ASM chart for dice game. 9

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